SSC8205GSB

Common Drain N-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
20V	±12V	18mR@4V5	6A
		22mR@2V5	

➢ Description

Advanced trench process technology. High density cell design for ultra-low on-resistance. High power and current handling capability. Fully characterized avalanche voltage and current.

➢ Applications

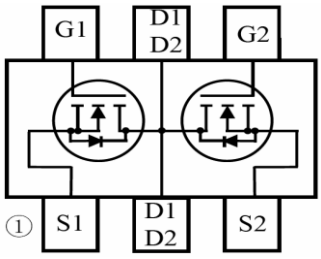
- Li-ion battery protection
- Load switch
- DCDC conversion

➢ Ordering Information

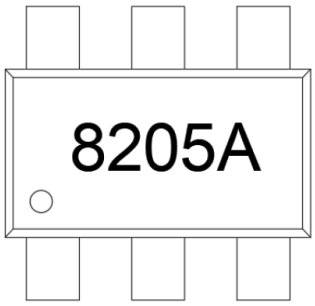
Device	Package	Shipping
SSC8205GSB	SOT23-6L	3000/Reel

➢ Pin configuration

Top view



SOT23-6L



➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	6	A
I_{DM}	Pulsed Drain Current [b]	18	A
P_D	Power Dissipation [c]	1.25	W
P_{DSM}	Power Dissipation [a]	0.7	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		190	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		105	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	20			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	0.5	0.65	1	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=4.5V,ID=3A		18	21	mR
		VGS=2.5V,ID=2A		22	25	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=16V,VGS=0V			1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=5V,ID=4.5A		10		S
V_{SD}	Forward Voltage	VGS=0V,IS=1.25A		0.8	1.3	V
Ciss	Input Capacitance	VDS=8V, VGS=0V, f=1MHz		600		pF
Coss	Output Capacitance			330		
Crss	Reverse Transfer Capacitance			140		
$T_{D(ON)}$	Turn-on delay time	VGEN=4.5V, VDS=10V, RG=6R,ID=1A		8		ns
Tr	Rise Time			10		
$T_{D(OFF)}$	Turn-off delay time			35		
Tf	Fall Time			30		
Qg	Total Gate charge	VGS=4.5V, VDS=10V, ID=6A		10		nC
Qgs	Gate to Source charge			2.3		
Qgd	Gate to Drain charge			2.9		

➢ Typical Characteristics(T_A=25℃ unless otherwise noted)

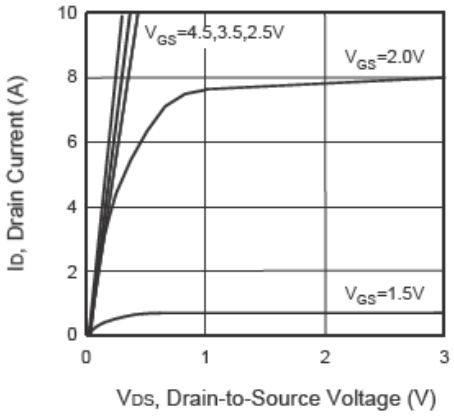


Figure 1. Output Characteristics

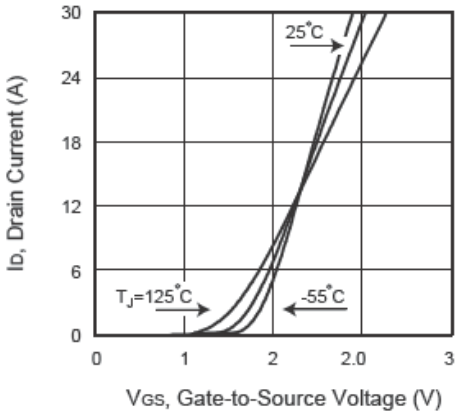


Figure 2. Transfer Characteristics

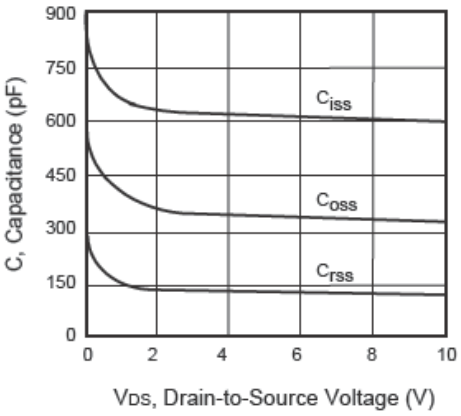


Figure 3. Capacitance

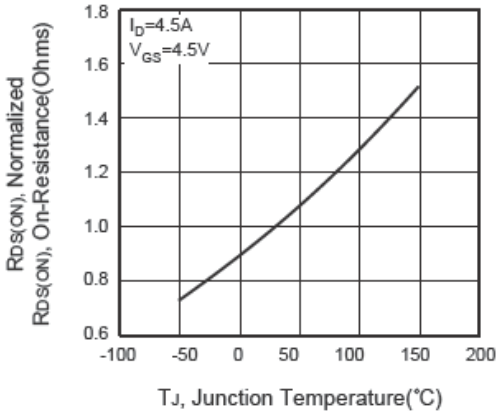


Figure 4. On-Resistance Variation with Temperature

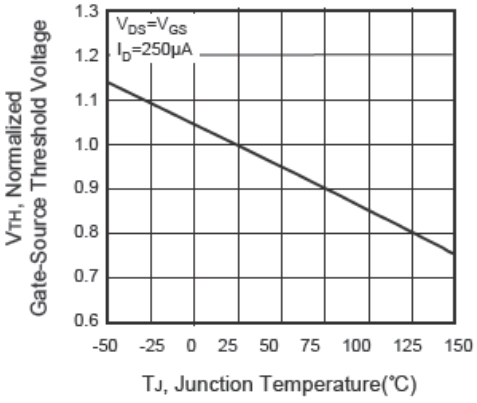


Figure 5. Gate Threshold Variation with Temperature

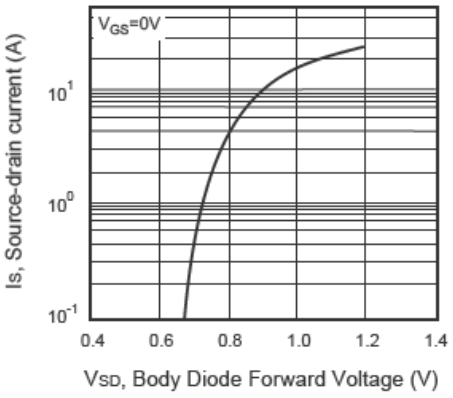


Figure 6. Body Diode Forward Voltage Variation with Source Current

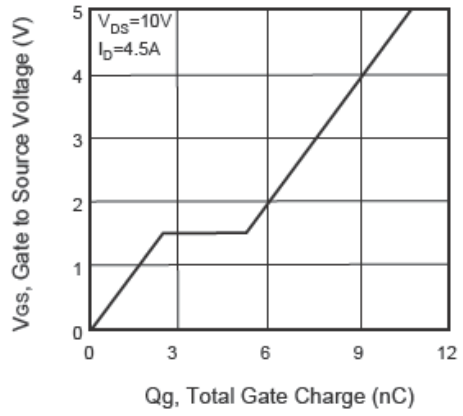


Figure 7. Gate Charge

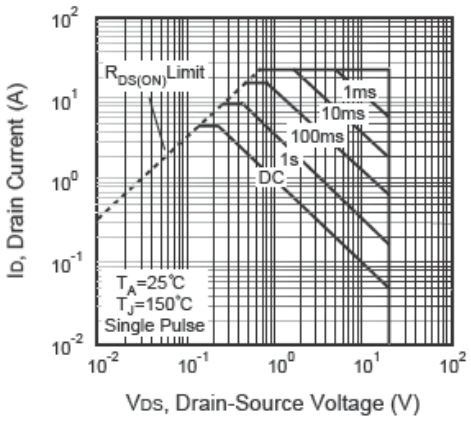


Figure 8. Maximum Safe Operating Area

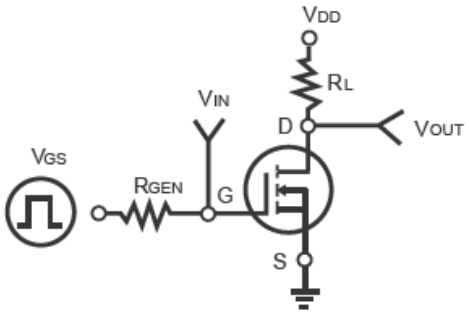


Figure 9. Switching Test Circuit

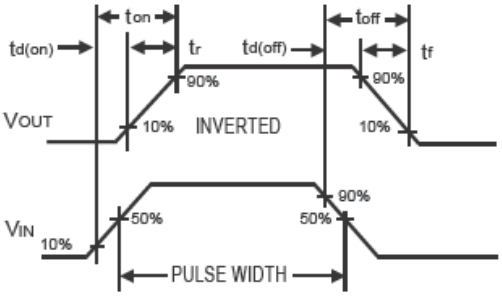


Figure 10. Switching Waveforms

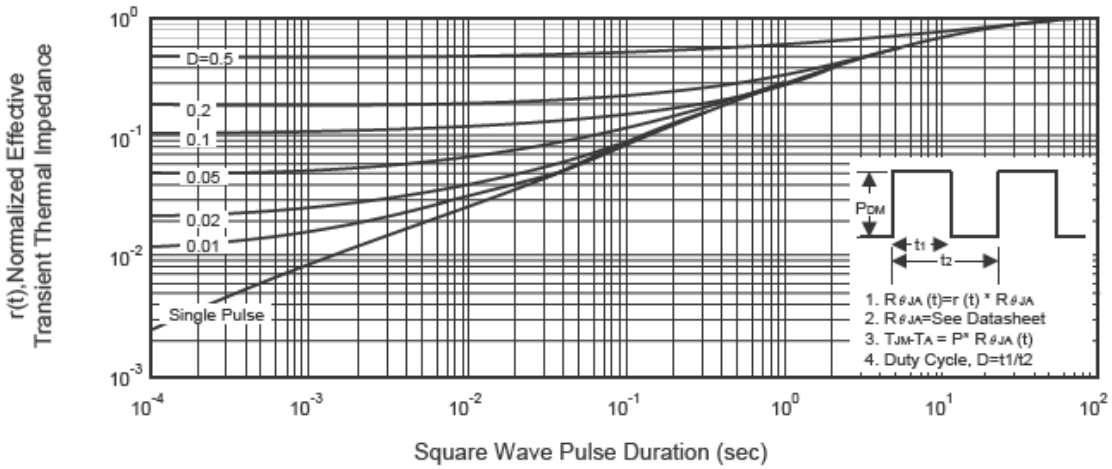
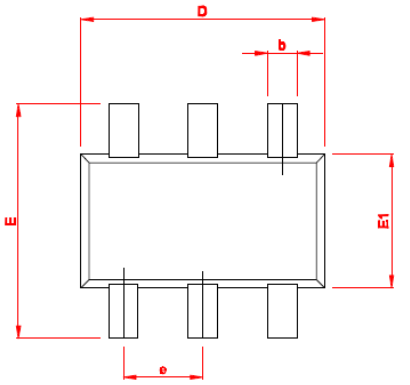
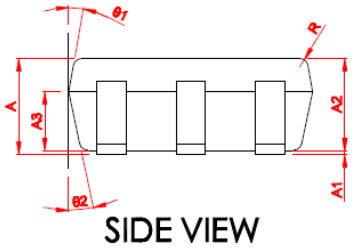


Figure 11. Normalized Thermal Transient Impedance Curve

➢ Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

➢ History Version

V1.0	Product datasheet	2020-01-17
V3.0	Update Typesetting	2020-07-24
V3.1	Increase Marking	2020-12-08

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